What is claimed is:

Claim 1. A multiprocessor computer system comprising,

a computer system having a plurality of processing nodes and caches and a node controller which use processor state information according to mappings provided by supervisor software or firmware of allowable physical processors to an application workload to determine which coherent cache regions in the system are required to examine a coherency transaction produced by a single originating processor's storage request.

Claim 2. The multiprocessor computer system according to claim 1 wherein a node of the computer has dynamic coherency boundaries such that the hardware uses only a subset of the total processors in the system for a single workload at any specific point in time and optimizes the cache coherency as the supervisor software or firmware expands and contracts the number of processors which are being used to run any single workload.

Claim 3. The multiprocessor computer system according to claim 1 wherein multiple instances of a node are connected with a second level controller to create a large multiprocessor system.

Claim 4. The multiprocessor computer system according to claim 1 wherein said node controller uses mode bits to determine which processors must receive any given transaction that is received by the node controller.

Claim 5. The multiprocessor computer system according to claim 1 wherein a second level controller is provided which uses the mode bits to determine which nodes must receive any

given transaction that is received by the second level controller.

Claim 6. The multiprocessor computer system according to claim 1 wherein logical partitions are provided and mapping of logical partitions to allowable physical processors is provided by provided by supervisor software or firmware of allowable physical processors to an application workload.

Claim 7. The multiprocessor computer system according to claim 1 wherein logical partitions are provided for the supervisor software or firmware which maps allowable physical processors to an application workload and a hypervisor assigns cache coherence regions which encompass subsets of the total number of processors and caches in the system chosen for their physical proximity and defines a distinct cache coherency region for each partition.

Claim 8. The multiprocessor computer system according to claim 1 wherein a single workload uses only a subset of the total processors in the computer system for a single workload at any specific point in time for an assigned partition and a distinct cache coherency is optimized for the address space of the assigned partition as the supervisor software or firmware expands and contracts the number of processors which are being used to run any single workload in said assigned partition.

Claim 9. The multiprocessor computer system according to claim 1 wherein a single workload uses only a subset of the total processors in the computer system for a single workload at any specific point in time, and

multiple cache coherent regions are assigned for different partitions as more independent workloads coexist on the same hardware.

Claim 10. The multiprocessor computer system according to claim 1 wherein cache coherence regions encompass subsets of the total number of processors and caches in the computer system and a single workload uses only a subset of the total processors in the computer system for a single workload at any specific point in time for an assigned partition and a distinct cache coherency is optimized for the address space of the assigned partition as the supervisor software or firmware expands and contracts the number of processors which are being used to run any single workload in said assigned partition.

Claim 11. The multiprocessor computer system according to claim 1 wherein software and/or firmware define which subset of processors in a large multiprocessor must participate in a coherency transaction independent of which processing node is connected to the physical DRAM storage being requested by said single originating processor.

Claim 12. The multiprocessor computer system according to claim 11 wherein the movement of a process between nodes of a large multiprocessor is effectuated without moving physical storage contents and without requiring subsequent broadcasting of the storage references originated by the process from said single originating storage request to all of the caches in the multiprocessor.

Claim 13. The multiprocessor computer system according to claim 1 wherein cache coherence mode bits are appended to a

processors storage transactions when transmitted to a connected processor of said multiprocessor computer system.

Claim 14. The multiprocessor computer system according to claim 13 wherein said cache coherence mode bits are used in a decision determining whether the single originating processor's storage request must be transmitted to additional processors in the system.

Claim 15. The multiprocessor computer system according to claim 14 wherein an increase in the effective utilization of the address bandwidth of the buses used to interconnect the processors of a multiprocessor system allows movement of workload among physical processors in a multiprocessor system at the same time as a reduction of the address bandwidth required to maintain cache coherency among all the processors.